



-84-

ABSTRACT OF THE DISCLOSURE

For erasing a block 0, a voltage Vpp is applied to select word lines WLO - WL31, while a voltage Vneg is applied to each of the substrate (well) and sub-bit lines SBL0 - SBL4096. Also, a voltage Vneg is applied to word lines WL32 - WL63 of a non-select block 1, while voltage Vneg is applied to the substrate (well) and the sub-bit lines SBL. Thus, the voltage Vneg is applied to the control gates, sources and drains of all the memory cells within the non-select block 1 and the substrate (well), so as to make them equal in voltage to one another. Therefore, there occur no mis-reads during the reading. Further, the capacity between the non-select word lines \mathtt{WL} substrate the (well) can be neglected, and occupancy ratio of the charge pump for use of supply of the negative voltage can be reduced by an extent corresponding to 90% or more of the conventional counterpart. mis-reads due to substrate disturb during the result, erasing can be prevented.

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